WHAT IS CLAIMED IS:

1. A solid state imaging device using N-type MOS transistors alone as transistors included therein, comprising:

a pixel unit composed of a plurality of pixels arranged in a two-dimensional matrix, each of said pixels including a photoelectric converting element for generating charge in response to light and an amplifying element for outputting, as an analog signal, a voltage signal corresponding to said charge generated by said photoelectric converting element;

a selection signal line provided correspondingly to each pixel row of said pixel unit;

a comparison/storage unit provided correspondingly to each pixel column of said pixel unit for converting, into a digital signal, said analog signal output from said amplifying element included in each pixel belonging to a pixel row selected in said pixel unit and for storing said digital signal;

a scanner for selecting and reading said digital signal stored in said comparison/storage unit in time series; and

an amplifier for amplifying said read digital signal and outputting said amplified digital signal to the outside.

2. The solid state imaging device of Claim 1,

wherein said comparison/storage unit includes a comparator, which includes three inverter circuits using N-type MOS transistors alone and serially connected to one another, and a booster circuit for preventing voltage attenuation of an output signal and accelerating said output signal,

in order to increase a fall speed of an inverter circuit disposed at the first stage out of said three inverter circuits, ON resistance of a transistor connected to GND potential is

set to be smaller than ON resistance of a transistor connected to power potential in said inverter circuit disposed at the first stage,

in order to increase a rise speed of an inverter circuit disposed at the second stage out of said three inverter circuits, ON resistance of a transistor connected to the power potential is set to be smaller than ON resistance of a transistor connected to the GND potential in said inverter circuit disposed at the second stage, and

in order to increase a fall speed of an inverter circuit disposed at the third stage out of said three inverter circuits, ON resistance of a transistor connected to the GND potential is set to be smaller than ON resistance of a transistor connected to the power potential in said inverter circuit disposed at the third stage.

3. The solid state imaging device of Claim 2,

wherein said comparison/storage unit includes a memory, which includes a first switch for reading a counter value on the basis of a signal supplied from said comparator, a capacitor for storing said read counter value, a second switch for transferring said counter value stored in said capacitor, a third switch for deleting said transferred counter value, a fourth switch for reading said transferred counter value on the basis of a signal supplied from said scanner, and said amplifier for outputting said read counter value to the outside, and

said amplifier includes a booster circuit for preventing voltage attenuation of an output signal thereof and accelerating said output signal.

4. The solid state imaging device of Claim 3, further comprising:

a pulse generator for generating a pulse signal on the basis of a column selection signal output from a horizontal scanner included in said scanner; and

a counter generator for generating said counter value on the basis of said pulse signal generated by said pulse generator.

5. The solid state imaging device of Claim 4,

wherein said counter generator includes a booster circuit for preventing voltage attenuation of an output signal thereof and accelerating said output signal.

6. The solid state imaging device of Claim 4, further comprising a ramp waveform generator for generating a ramp signal on the basis of said pulse signal generated by said pulse generator and said counter value generated by said counter generator.

7. A solid state imaging device, comprising:

a pixel unit formed on a semiconductor substrate and outputting, as an analog signal, a voltage signal corresponding to light; and

an AD converter formed on said semiconductor substrate and converting said analog signal output from said pixel unit into a digital signal,

wherein transistors included in said pixel unit and said AD converter are all N-type MOS transistors, and

said AD converter includes a booster circuit.

8. The solid state imaging device of Claim 7,

wherein said booster circuit includes a transistor whose source or drain is connected to power potential, and

a voltage not less than said power potential is applied to a gate of said transistor.

9. The solid state imaging device of Claim 7,

wherein said AD converter includes, in addition to said booster circuit, any or all of a comparator, a memory, a pulse generator and a counter generator.

10. The solid state imaging device of Claim 9,

wherein said comparator includes an inverter circuit having said booster circuit,

said booster circuit includes a first transistor whose source or drain is connected to

power potential, and

a voltage not less than said power potential is applied to a gate of said first transistor.

11. The solid state imaging device of Claim 9,

wherein said comparator includes an inverter circuit having said booster circuit,

said inverter circuit has a second transistor formed above a well region independent of other well regions, and

a gate and a source of said second transistor are electrically connected to said well region.

12. The solid state imaging device of Claim 9,

wherein said memory includes a plurality of switches, a capacitor and an output amplifier,

said output amplifier includes a booster circuit,

said booster circuit has a transistor whose source or drain is connected to power potential, and

a voltage not less than said power potential is applied to a gate of said transistor.

13. The solid state imaging device of Claim 12, further comprising a scanner for selecting and reading a digital signal obtained by said AD converter in time series,

wherein said memory includes a first switch for reading a counter value on the basis of a signal supplied from said comparator, a capacitor for storing said read counter value, a second switch for transferring said counter value stored in said capacitor, a third switch for deleting said transferred counter value, a fourth switch for reading said transferred counter value on the basis of a signal supplied from said scanner, and an output amplifier for outputting said read counter value to the outside.

14. The solid state imaging device of Claim 9, further comprising a scanner for

selecting and reading a digital signal obtained by said AD converter in time series,

wherein said pulse generator generates a pulse signal on the basis of a column selection signal output from a horizontal scanner included in said scanner and includes a plurality of inverter circuits serially connected to one another,

an inverter circuit disposed at the ultimate stage out of said plurality of inverter circuits includes a booster circuit,

said booster circuit has a transistor whose source or drain is connected to power potential, and

a voltage not less than said power potential is applied to a gate of said transistor.

15. The solid state imaging device of Claim 9,

wherein said counter generator generates a counter value on the basis of a pulse signal generated by said pulse generator and includes a plurality of inverter circuits each having a booster circuit,

said booster circuit has a transistor whose source or drain is connected to power potential, and

a voltage not less than said power potential is applied to a gate of said transistor.